Soft USB Design Challenges

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Soft USB Design Challenges
The Objective: **SOFT**

- Enhanced 8051 Core
- 3.3V, 24 MHz, 4-clock cycle
- Program and Data RAM
- USB Function Traffic
- I/O

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The diagram illustrates the system architecture with a clear focus on the Enhanced 8051 Core, which operates at 3.3V and 24 MHz with a 4-clock cycle. The system includes program and data RAM, USB function traffic, and an I/O interface.
The Basic USB Interface

Serial Interface Engine (SIE)

Bytes

USB Transceiver
What the SIE Does

Serial Interface Engine (SIE)

USB Tranceiver

Payload Data

ACK

Payload Data

ACK
A USB Control Transfer
EZ-USB Enhanced SIE

Anchor Chips Enhanced SIE

Serial Interface Engine (SIE)

Full Device Enumeration

intelligence
## Default Endpoints

<table>
<thead>
<tr>
<th>Endpoint</th>
<th>Type</th>
<th>Alternate Setting</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Max Packet Size (bytes)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>CTL</td>
<td>64</td>
</tr>
<tr>
<td>1 IN</td>
<td>INT</td>
<td>0</td>
</tr>
<tr>
<td>2 IN</td>
<td>BULK</td>
<td>0</td>
</tr>
<tr>
<td>2 OUT</td>
<td>BULK</td>
<td>0</td>
</tr>
<tr>
<td>4 IN</td>
<td>BULK</td>
<td>0</td>
</tr>
<tr>
<td>4 OUT</td>
<td>BULK</td>
<td>0</td>
</tr>
<tr>
<td>6 IN</td>
<td>BULK</td>
<td>0</td>
</tr>
<tr>
<td>6 OUT</td>
<td>BULK</td>
<td>0</td>
</tr>
<tr>
<td>8 IN</td>
<td>ISO</td>
<td>0</td>
</tr>
<tr>
<td>8 OUT</td>
<td>ISO</td>
<td>0</td>
</tr>
<tr>
<td>9 IN</td>
<td>ISO</td>
<td>0</td>
</tr>
<tr>
<td>9 OUT</td>
<td>ISO</td>
<td>0</td>
</tr>
<tr>
<td>10 IN</td>
<td>ISO</td>
<td>0</td>
</tr>
<tr>
<td>10 OUT</td>
<td>ISO</td>
<td>0</td>
</tr>
</tbody>
</table>
Advanced SIE Enumerates & Loads Code

Anchor Chips
Enhanced SIE

Serial Interface Engine (SIE)

intelligence

Enhanced 8051 Core
3.3V, 24 MHz, 4-clock cycle

Program and Data RAM

Full Device Enumeration

Download & Upload Code
The Download Request

<table>
<thead>
<tr>
<th>Byte</th>
<th>Field</th>
<th>Value</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>bmRequest</td>
<td>0x40</td>
<td>Vendor Request, OUT</td>
</tr>
<tr>
<td>1</td>
<td>bRequest</td>
<td>0xA0</td>
<td>“Anchor Load”</td>
</tr>
<tr>
<td>2</td>
<td>wValueL</td>
<td>AddrL</td>
<td>Starting address</td>
</tr>
<tr>
<td>3</td>
<td>wValueH</td>
<td>AddrH</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>wIndexL</td>
<td>0x00</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>wIndexH</td>
<td>0x00</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>wLengthL</td>
<td>LenL</td>
<td>Number of Bytes</td>
</tr>
<tr>
<td>7</td>
<td>wLengthH</td>
<td>LenH</td>
<td></td>
</tr>
</tbody>
</table>
Final USB Device

Anchor Chips Enhanced SIE

Serial Interface Engine (SIE)

Enhanced 8051 Core
3.3V, 24 MHz, 4-clock cycle

Program and Data RAM

I/O

USB Function Traffic
AN2131Q Memory Map

EZ-USB regs
Endpoint 0 IN
Endpoint 0 OUT
Endpoint 1 IN
Endpoint 1 OUT
Endpoint 2 IN
Endpoint 2 OUT
Endpoint 3 IN
Endpoint 3 OUT
Endpoint 4 IN
Endpoint 4 OUT
Endpoint 5 IN
Endpoint 5 OUT
Endpoint 6 IN
Endpoint 6 OUT
Endpoint 7 IN
Endpoint 7 OUT

6.5K RAM

1024 Bytes Isochronous FIFOS

1024 Bytes Isochronous FIFOS

1024 bytes Bulk Endpoint Buffers

1B40

0000

2000

1F3F

SOF

All 31 USB endpoints are available

USB endpoints:
- Endpoint 0 control
- Endpoints 1-7 bulk/interrupt
- Endpoints 8-15 isochronous

USB
Enumeration

Host PC recognizes device attachment, starts Enumeration process

EZ-USB Core provides device descriptors to identify the loader driver.

Host PC loads loader driver, which loads firmware and descriptors into device from a software file

Host PC

Your Peripheral Device
The ReNumeration™ Process

Host PC recognizes device attachment, starts Enumeration process.

Host PC loads loader driver, which loads firmware and descriptors into device from a software file.

Host PC Enumerates again, loads device driver.

EZ-USB Core provides device descriptors to identify the loader driver.

Final USB device. EZ-USB CPU services USB and provides device functionality.

The Magic Happens

Your Peripheral Device
Emulating a Physical Disconnect
Using the Enhanced SIE

Anchor Chips
Enhanced SIE

Serial Interface Engine (SIE)

Enhanced 8051 Core
3.3V, 24 MHz, 4-clock cycle

Program and Data RAM

I/O

USB Function Traffic
Get Descriptor—Without Enhanced SIE

1. USB Setup data copied to FIFO
2. CPU copies FIFO data to RAM, decodes “Get Descriptor” Request
3. CPU transfers first packet of data from memory to endpoint FIFO.
4. FIFO Data sent in response to USB IN token
5. CPU Transfers next packet of data from memory to endpoint FIFO.
6. FIFO Data sent in response to USB IN token
7. Repeat steps 5–6 as necessary.
Get Descriptor--With Enhanced SIE

1. EZ-USB core copies Setup data directly to RAM, eliminating the FIFO-to-RAM copy step. 8051 decodes the "Get Descriptor" request.

2. 8051 sets pointer to descriptor table in RAM, EZ-USB core does entire multi-packet transfer.
Watch Those VID-PID-DIDs

(a) "Anchor Generic" Enumeration

PC
Loads Anchor Chips Driver

EZ-USB

Vendor ID (VID)
Product ID (PID)
Device ID (DID)

(b) Custom Device Enumeration

PC
Loads Device-Specific Driver

EZ-USB

Serial EEPROM
IO Bandwidth Is Important

```
movx a,@dptr
D[7..0]
movx @dptr,a
```

```
FWR#
```

```
External FIFO or ASIC
```
AN2131 Transfers to External FIFO

2: USB D+  0: FRD# strobes  1: FWR# strobes  15-8 D[7-0].
ISO transfer to endpoint 8 OUT, 1008 bytes of incrementing counter.
1008 data bytes transferred to external FIFO using 1008 FWR# strobes,
then transferred into EP8IN buffer using 1008 FRD# strobes. 2016 bytes are
transferred out of/into AN2131Q in about 700ns or 70% of the frame time.
Expanding the AN2131Q

- PORTA (8)
- PORTB (8)
- PORTC (8)
- Address (16)
- Data (8)
- I²C

Alternate Function:
- OE
- OUT
- PIN

Diagram showing the connection between AN2131Q and Pin with I²C and other ports.
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